REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 3 through 12, and 14 through 22, are now in this case. Claims 1, 2, and 13 are canceled. Claims 7, 11, 12, 14, and 17 through 19 are amended. Claims 21 and 22 are added.

Claims 3 through 6 stand allowed. Claims 7 through 10 and 14 through 20 were objected to because of certain informalities, but were indicated as directed to patentable subject matter. Claims 1, 14, and 17 through 19 are amended as suggested by the Examiner, which Applicant respectfully submits overcomes the objection to these claims.

Claims 1 and 2 were rejected under §103 as unpatentable over the Baron et al. reference[1] in view of the Tanenbaum reference[2]. Claims 1 and 11 were also rejected under §103 as unpatentable over the Nakagawa et al. reference[3], in view of the combination of the Baron et al. and Tanenbaum references.[4]

Claims 1 and 2 are canceled to advance the prosecution of this case. Claim 11 is amended to now depend on claim 3, which stands allowed as noted above.

Claims 12 and 13 are rejected under §103 as unpatentable over the Baron et al. reference in view of the Tanenbaum reference. The Examiner asserted that the Baron et al. reference teaches all of the elements of claim 12 except for the specifics of the DMA transfer, which the Examiner found to be taught by Tanenbaum; the Examiner further asserted that the skilled

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[1] U.S. Patent No. 5,586,293, issued December 17, 1996 to Baron et al.
[2] Tanenbaum, *Modern Operating Systems* (Prentice-Hall, 1992), pp. 208-10.
[3] U.S. Patent No. 6,643,713 B2, issued November 4, 2003 to Nakagawa et al. But more properly, for the reasons set forth in the Amendment of February 17, 2004, citation should be made to the parent of the Nakagawa et al. reference, which is U.S. Patent No. 6,353,863, issued from application S.N. 09/051,286, filed as a PCT application PCT/JP96/02910, or to the apparent PCT publication WO97/14093, published April 17, 1997.
[4] Office Action, *supra*, pages 5 and 6, ¶8.

artisan would have obviously combined the DMA transfer operation from Tanenbaum into the Baron et al. system to free the CPU from low-level work.[5]

Claim 12 is amended to overcome the rejection. The method of amended claim 12 now recites the steps of transferring a block of data values from a second memory to the local memory using a direct memory access controller, and responsive to transferring a data value to one of the segments in the local memory, setting its indicator bit to a valid state. The method further recites the operating of the processor to access a selected segment in the local memory and, responsive to the state of the indicator bit for that segment not being in its valid state, operating the direct memory access controller to transfer the selected segment in the local memory. The specification clearly supports this amendment to claim 12,[6] and as such no new matter is presented by this amendment.

The method of amended claim 12 provides important advantages in the operation of a digital system. In particular, this system provides the important advantages of providing a local memory for a processor, especially in a multiple-processor system, in which data may be transferred to the local memory by DMA, and in which processor and DMA access to the local memory is readily coordinated.

Claim 13 is canceled, obviating its rejection.

Applicant respectfully submits that amended claim 12 is patentably distinct over the prior art of record in this case, because the combined teachings of the prior art fall short of the requirements of the claim.

Nowhere does the Baron et al. reference anywhere disclose the step of operating a direct memory access controller to transfer a data value to a selected segment in a local memory, responsive to the state of an indicator bit associated with the selected segment, as accessed by the processor, not being in its valid state as required by claim 12. Rather, the cited location of the Baron et al. reference merely indicates that the valid bits are considered in CACHE MODE,

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[5] Office Action of December 13, 2002, pages 3 and 4, ¶5.

[6] Specification, *supra*, paragraphs 41 through 44; paragraphs 63 through 67; paragraphs 81 through 85.

after the loading of the internal program RAM in the PRAM MODE.[7] Presumably, an access of this memory in CACHE MODE results in the processor itself then accesses main memory to obtain the desired memory contents, according to conventional cache memory operation (and depending on whether there is a cache tag match to the desired address).[8] But the reference does not disclose that the DMA controller of the system effects this transfer in the result of an invalid indicator bit, as required by the method of claim 12. Accordingly, Applicant submits that amended claim 12 is novel over the Baron et al. reference.

The other references of record, including the Tanenbaum and Nakagawa et al. references applied against the claims, add no teachings regarding this method step. Accordingly, Applicant submits that the combined teachings of the references fall short of the requirements of amended claim 12.

Applicant further respectfully submits that there is no suggestion from the prior art to modify these teachings in such a manner as to reach amended claim 12. Starting with the Baron et al. reference, this lack of suggestion is especially apparent, considering that the loading of the memory and its subsequent access are disclosed as occurring in two separate operating modes (*i.e.*, the PRAM MODE and the CACHE MODE), as determined by the state of a CACHE ENABLE bit in an operating mode register.[9] In contrast, the method of amended claim 12 is directed to the smooth and seamless cooperation of a processor and its local memory, operating in cooperation with a DMA controller that effects block transfers to that local memory. The claimed method provides a way that the DMA controller can effect its block transfer, while also remaining available for transferring data, into the local memory, on demand of the processor. Again, the other references of record in this case provide no suggestion in this regard. Considering the important advantages provided by the inventive method of claim 12, Applicant respectfully submits that amended claim 12 and its dependent claims are patentably distinct over the prior art of record in this case.

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[7] Baron et al., *supra*, column 8, lines 27 through 36.
[8] *See* Baron et al., *supra*, column 5, line 53 through column 6, line 16.
[9] Baron et al., *supra*, column 4, lines 12 through 21.

Claims 21 and 22 are added to more completely cover all aspects of Applicant's invention.

Specifically, new claim 21 further requires, relative to amended claim 12 upon which it depends, the step of starting the transferring of the block of data values, using the direct memory access controller, after the operating of the direct memory access controller to transfer the data value into the selected segment in the local memory that occurred in response to the access of this segment by the processor, but with the indicator bit for that segment not being valid. The specification clearly supports this additional step in connection with an alternative implementation in which this operation initiates the block transfer,[10] and as such no new matter is presented by this new claim 21.

New claim 22 further requires, relative to claim 12 upon which it also depends, that the step of operating the processor is performed during the block transferring step and, responsive to the state of the indicator bit for a segment addressed by the processor not being valid, the step of halting the transferring step; the method of claim 22 further requires the restarting of the transferring step after the data value has been transferred to the selected segment. The specification clearly supports this new method,[11] and as such no new matter is presented by this new claim 22.

In addition to the reasons discussed above relative to amended claim 12, upon which new claims 21 and 22 depend, Applicant submits that these new claims 21 and 22 are further patentably distinct over the prior art of record. There is no disclosure, in any of the references, of the starting of the transferring of a block of data values after the direct memory access controller has transferred the addressed segment to the local memory, as required by claim 21. And there is also no disclosure, in any of the references, of the simultaneous DMA and processor access to a local memory, much less the halting of the DMA transferring and its restarting after the transfer of the data value to the selected segment (for which the indicator bit was not valid), as required by claim 22.

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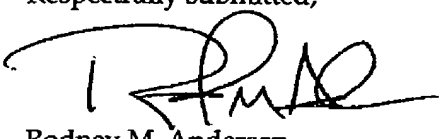
[10] Specification, *supra*, paragraph 67.
[11] Specification, *supra*, paragraph 66.

Because the prior art of record falls even further short of the requirements of these new claims, Applicant submits that these claims are further patentably distinct over the prior art of record in this case.

Attention is directed to the Information Disclosure Statement that the undersigned understands, on information and belief, to have been filed in this application on or about July 13, 2004. Consideration of that information is again requested.

For the reasons discussed above, Applicant submits that all claims now in this case are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,



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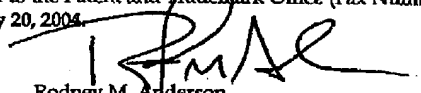

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